PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
B24B 7/22, 23/02, B24C 1/04, 1/08

A1

(11) International Publication Number: **WO 99/46081**

(43) International Publication Date: 16 September 1999 (16.09.99)

(21) International Application Number: PCT/US99/05192

(22) International Filing Date: 10 March 1999 (10.03.99)

(30) Priority Data:

60/077,569	11 March 1998 (11.03.98)	US
09/265,771	10 March 1999 (10.03.99)	US

(71) Applicant: STRASBAUGH [US/US]; 825 Buckley Road, San Luis Obispo, CA 93401 (US).

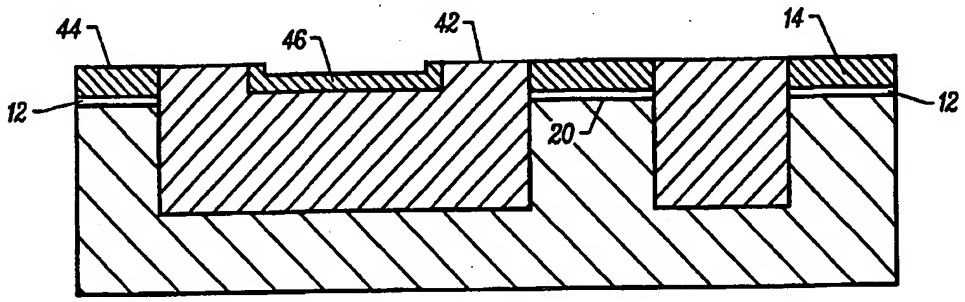
(72) Inventor: BOYD, John, M.; 9182 Tiburon Circle, Atascadero, CA 93422 (US).

(74) Agents: OGAWA, Richard, T. et al.; Townsend and Townsend and Crew LLP, 8th floor, Two Embarcadero Center, San Francisco, CA 94111-3834 (US).

(81) Designated States: DE, GB, JP, KR.

Published
With international search report.

(54) Title: MULTI-STEP CHEMICAL MECHANICAL POLISHING PROCESS AND DEVICE



(57) Abstract

A technique for chemical mechanical polishing is provided. The technique uses a plurality of polishing tables to selectively remove films overlying semiconductor substrates. For instance, the technique relies upon a step of partially planarizing on a first CMP table a layer of chemical mechanical polish resistant material (22) using a first CMP step by selective removal of a chemical mechanical polish resistant material (22) overlying a non-uniform film (42). The technique also uses a second step of planarizing on a second CMP table to complete planarizing the non-uniform film (42). The combination of these steps often prevents microscratching of the film underlying the chemical mechanical polish resistant material and provides a substantially uniform polished film without dishing.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AL	Albania	**ES**	Spain	**LS**	Lesotho	**SI**	Slovenia
AM	Armenia	**FI**	Finland	**LT**	Lithuania	**SK**	Slovakia
AT	Austria	**FR**	France	**LU**	Luxembourg	**SN**	Senegal
AU	Australia	**GA**	Gabon	**LV**	Latvia	**SZ**	Swaziland
AZ	Azerbaijan	**GB**	United Kingdom	**MC**	Monaco	**TD**	Chad
BA	Bosnia and Herzegovina	**GE**	Georgia	**MD**	Republic of Moldova	**TG**	Togo
BB	Barbados	**GH**	Ghana	**MG**	Madagascar	**TJ**	Tajikistan
BE	Belgium	**GN**	Guinea	**MK**	The former Yugoslav Republic of Macedonia	**TM**	Turkmenistan
BF	Burkina Faso	**GR**	Greece			**TR**	Turkey
BG	Bulgaria	**HU**	Hungary	**ML**	Mali	**TT**	Trinidad and Tobago
BJ	Benin	**IE**	Ireland	**MN**	Mongolia	**UA**	Ukraine
BR	Brazil	**IL**	Israel	**MR**	Mauritania	**UG**	Uganda
BY	Belarus	**IS**	Iceland	**MW**	Malawi	**US**	United States of America
CA	Canada	**IT**	Italy	**MX**	Mexico	**UZ**	Uzbekistan
CF	Central African Republic	**JP**	Japan	**NE**	Niger	**VN**	Viet Nam
CG	Congo	**KE**	Kenya	**NL**	Netherlands	**YU**	Yugoslavia
CH	Switzerland	**KG**	Kyrgyzstan	**NO**	Norway	**ZW**	Zimbabwe
CI	Côte d'Ivoire	**KP**	Democratic People's Republic of Korea	**NZ**	New Zealand		
CM	Cameroon			**PL**	Poland		
CN	China	**KR**	Republic of Korea	**PT**	Portugal		
CU	Cuba	**KZ**	Kazakstan	**RO**	Romania		
CZ	Czech Republic	**LC**	Saint Lucia	**RU**	Russian Federation		
DE	Germany	**LI**	Liechtenstein	**SD**	Sudan		
DK	Denmark	**LK**	Sri Lanka	**SE**	Sweden		
EE	Estonia	**LR**	Liberia	**SG**	Singapore		

MULTI-STEP CHEMICAL MECHANICAL POLISHING PROCESS AND DEVICE

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority to U.S. Serial No. 60/077,569 filed March 11, 1998 (Attorney Docket No. 17074-000800) and U.S. Serial No. _____, filed March 10, 1999 (Attorney Docket No. 17074-000810), which are hereby incorporated by reference for all purposes.

BACKGROUND OF THE INVENTION

This invention relates to a method of fabricating integrated circuits. More particularly, the present invention provides a planarization technique by way of chemical mechanical polishing or planarization.

In the fabrication of conventional VLSI and ULSI integrated circuits, various planarization techniques have been proposed. A fully recessed isolation technique, typically know as "shallow trench isolation" or "STI", is being used in submicron manufacturing processes. This isolation technique reduces the variation in surface topography and tends to help eliminate process and device integration problems associated with techniques such as "local oxidation of silicon" (LOCOS) which often produce less-planar surfaces. Another technique uses fully planar dielectrics to isolate multiple levels of metal interconnect materials, known as an "interlevel dielectric" or "ILD". In general, planar topography is often required to reduce depth of focus budget as well as improve reliability and interconnect linewidth control.

Further techniques used to planarize films on wafers in an integrated circuit fabrication process include:

1. Block resist and resist etch back;
2. Block resist, reactive ion etch and chemical mechanical polishing;
3. Spin-on glass and reactive ion etch;
4. Various combinations of 1-3; and
5. "Dummy features" made during the lithographic process and chemical mechanical polishing.

Still a further technique which offers a relatively simple and effective method of planarization is chemical mechanical polishing, commonly termed CMP. CMP

can provide effective planarization without additional masking or coating steps. A difficulty encountered using CMP, however, is pattern sensitivity. Pattern sensitivity causes difficulty in effectively planarizing large dense features without "dishing" in low regions. Dishing often occurs in both STI planarization as well as ILD planarization. Dishing is particularly severe in DRAM IC manufacturing processes where very dense regions in the memory cell array region are planarized simultaneously with significantly less dense regions in the peripheral circuitry.

Another limitation associated with CMP is "microscratching" of the dielectric regions, which is introduced during the CMP process. Microscratching is increasingly a concern in the fabrication of submicron-sized (i.e., 0.25 μm and less) devices which use CMP planarization. Accordingly, CMP is severely limited for today's state-or-art devices.

A further limitation associated with some of the above processes is a resultant step height differential of the field oxide and device well (active area) beneath the gate electrode regions. If the resultant field oxide surface under the gate electrode is below the planar substrate surface, the gate dielectric thickness is reduced in the corner region produced by the intersection of the trench sidewall and the planar substrate surface, by a phenomenon known as stress-induced oxidation retardation. This can cause lowering of the transistor threshold voltages, degradation of the sub-threshold characteristics, and early breakdown or wear out of the gate dielectric. Moreover, additional problems occur using multi-slurry processing in CMP which can cross-contaminate slurry mixtures, thereby causing damage to integrated circuit devices.

From the above, it is seen that a technique for planarizing films in integrated circuits that is easy and effective is highly desirable.

SUMMARY OF THE INVENTION

The present invention provides a method of planarizing films in integrated circuits using chemical mechanical polishing. In an exemplary embodiment, the present invention uses multi-table polishing tools to perform multi-step polishing processes to improve uniformity and quality of a film. See, for example, U.S. Serial No. _____ (Attorney Docket No. 17074-000220), commonly assigned and which is hereby incorporated by reference for all purposes.

According to one aspect of this invention, a method is provided for fabricating an integrated circuit. The method includes steps of providing a semiconductor

substrate having a planar surface and comprising a surface layer of a protective material which prevents damage to the underlying substrate during the CMP process step, the substrate having defined therein a steep-sided trench, filling the trench with at least one conformal layer of a trench filling material and a conformal layer of chemical mechanical polish resistant material, the layer of chemical mechanical polish resistant material within the trench providing, in a center region of the trench a polish stop (e.g., silicon nitride, boron nitride, boron saturated polysilicon (10^{20-22} ions of boron/cm^3, silicon carbide, nitrided oxides, titanium nitride, tungsten, metals, refractory metals, or any other material that is relatively harder than the underlying film) having a surface higher than the surface layer of chemical mechanical polish resistant material of the semiconductor substrate; and planarizing the resulting structure by a two-step chemical mechanical polishing. The first step is carried out on a first dedicated polish platen that selectively removes the polish resistant material above the conformal layer of trench filling material in the regions not subtended by the trench by a high-speed low-down force polish process. The second step is carried out on a second dedicated polish platen, which selectively removes the trench filling material above the protective material in the regions not subtended by the trench by a conventional lower-speed, high down force polish process, thereby selectively removing layers extending above the planar surface of the substrate and the protective material.

Thus, dishing is avoided in the wider trenches during chemical mechanical polishing by the two-step selective process, the conformal polish resistant material providing a polish stop in the central region of the trench due to a combination of at least the first-speed polish process, and the very high selectivity during the second polish step of the conformal trench fill material to the polish resistant material. In a specific embodiment, a different slurry mixture is used in each of the polishing processes. By way of using a multi-table process, where each table has a different slurry type, the two slurry types are prevented from cross-contaminating each other in a multi-step process. Accordingly, enhanced control of the process can be achieved. A further rinsing step could be incorporated as an intermediate process step between the first and second table processes to further avoid cross-contamination of slurries. The rinsing step removes any residual slurry material (e.g., abrasive, solvent, liquid) that may be attached to surfaces of the substrate from the first polishing process.

Preferably, the thickness of the chemical mechanical polish resistant material is significantly thinner than the protective material in order to allow it's selective removal during the first polish step thus allowing exposure of the conformal fill

material above the protective layer without exposing the conformal fill material in the trench regions. Additionally, the thickness of the polish resistant layer, the depth of the trench and the thickness of the conformal trench fill material are selected so that after removal of the polish resistant layer and the trench fill layer above the regions not subtended by the trenches, and subsequent processing to remove the polish resistant material and form the gate electrodes, the resultant field oxide surface is slightly higher than the surface of the planar substrate.

Thus, dishing is avoided in the wider trenches during chemical mechanical polishing by the two-step selective process, the conformal polish resistant material providing a polish stop in the central region of the trench due to the very high selectivity during the second polish step of the conformal trench fill material to the polish resistant material.

An alternative embodiment provides a very hard polish pad on the first table during the first step of the two-step process, thereby eliminating a need for a high speed, low pressure polish step, and a soft pad can be used on the second table during the second step of the two-step process. Further variations, alternatives, and modifications can be also employed without departing from the spirit and scope of the invention.

According to another aspect of the present invention, a method of fabricating an integrated circuit using a multi-step CMP process is provided. The method includes, among others, a step of providing a semiconductor substrate having formed thereon a conductive layer and an overlying dielectric layer having a non-planar surface. A step of forming a conformal layer of chemical mechanical polish resistant material overlying the dielectric layer is included. The resultant structure is planarized by at least a two-step chemical mechanical polishing. The first step selectively removes the polish resistant material above the dielectric layer overlying the conductive layer, and the second step selectively removes the dielectric layer above the conductive layer until the dielectric layer and the polish resistant layer in regions not overlying the conductive layer are coplanar, thereby selectively removing layers extending above the conductive layer.

Thus, dishing is avoided in the regions not subtended by the conductive layer during chemical mechanical polishing by the two-step selective process, the conformal polish resistant material providing a polish stop (e.g., silicon nitride, boron nitride, boron saturated polysilicon (10^{20-22} ions of boron/cm^3, silicon carbide, nitrided oxides, titanium nitride, tungsten, metals, refractory metals, or any other material that is relatively harder than the underlying film) in the central region of the trench due to the

very high selectivity during the second polish step of the conformal trench fill material to the polish resistant material.

According to yet another aspect of the present invention, there is provided a method of fabricating an integrated circuit comprising: providing a semiconductor substrate having formed thereon a conductive layer; patterning the conductive layer and forming an overlying dielectric layer; planarizing the overlying dielectric layer; forming trenches in the dielectric layer; providing openings in the trenches exposing the underlying conductive layer; forming a second conductive layer which may be comprised of one or more layers of conductive material; providing a conformal layer of chemical mechanical polish resistant material overlying the second conductive layer, and planarizing the resulting structure by a two-step chemical mechanical polishing in which the first step selectively removes the polish resistant material above the second conductive layer overlying the second dielectric and first conductive layers, and the second step selectively removes the conductive layer above the second conductive layer until the dielectric layer and the polish resistant layer in regions not overlying the conductive layer are coplanar, thereby selectively removing layers extending above the second dielectric layer.

Thus, dishing is avoided in the regions no subtended by the second dielectric layer during chemical mechanical polishing by the two-step selective process, the conformal polish resistant material providing a polish stop in the central region of the trench due to the very high selectivity during the second polish step of the second conductive layer to the polish resistant material.

In an alternative embodiment, the present invention provides a method for planarizing a film of material on a substrate structure. The method includes providing a substrate comprising a top surface and a film to be polished overlying the top surface. The method also includes removing a first portion of the film using a first polishing table; and removing a second portion of the film using a second polishing table to selectively remove the second portion of the film relative to the top surface. Preferably, the first polishing table and the second polishing table are provided on a common platform to improve efficiency in processing.

Numerous advantages are achieved using the present invention over conventional techniques. In particular, the present invention can avoid limitations encountered by Boyd et al., U.S. Patent No. 5,362,669, in which the thickness of the conformal polish resistant material is equivalent to the thickness of the protective material

and the surface of the conformal polish resistant material is co-planar with the surface of the protective material. This generally severely limits the usefulness of the invention in Boyd et al. to a shallow trench isolation process and may make it completely unusable. It is critical that the thickness of the protective material is sufficient not only to protect the substrate regions from the CMP process but also to provide a suitable step height differential between the field upon completion of the post-planarization process steps typically required in a fully-integrated IC process sequence. Additionally, it is critical that the conformal polish resistant material is thin enough to allow selective removal in the regions not subtended by the trench region. Finally, his invention does not allow it's use for planarization of ILD layers. These and other benefits are described throughout the present specification and more particularly below.

The present invention achieves these benefits in the context of known process technology. However, a further understanding of the nature and advantages of the present invention may be realized by reference to the latter portions of the specification and attached drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will now be described by way of example, with reference to the accompanying drawings, in which:

Figs. **1** to **6** show schematic cross-sectional views of part of a partially fabricated integrated circuit structure at successive stages in forming a trench isolation region according to a first embodiment of the present invention;

Figs. **7** to **10** show schematic cross-sectional views a partially fabricated integrated circuit structure at successive stages in forming an interconnect with planarized ILD according to a second embodiment of the present invention; and

Figs. **11** to **14** show a simplified pictorial of experiments according to the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

In a method of forming an integrated circuit according to a first embodiment of the present invention, as shown in Figs. 1 to 6, a substrate for an integrated circuit is provided in the form of a P type, <100> semiconductor silicon wafer **10**, as shown in Fig. 1. The substrate wafer is provided with a first layer **12** of a stress relief material, e.g. silicon dioxide, and an overlying layer of a chemical mechanical

polish resistant material **14** e.g. silicon nitride, boron nitride or other effective CMP resistant material to provide a selective polish stop.

Trench isolation regions **16** and **18** are defined on the substrate e.g. by a conventional photoengraving step involving coating with photoresist, and patterning. Trenches **16** and **18** are formed in the substrate **10** by a conventional known method of anisotropic etching.

Subsequently a conformal layer **42** of a dielectric material is deposited overall to fill the trenches **16** and **18** (Fig. 2). The dielectric comprises for example a conformal layer of CVD silicon dioxide. The thickness of the layer is sufficient to fill the wider trench **18** to a level above the substrate surface layer **20** and completely fills the narrower trenches **16**. The second dielectric layer **42** extends over the polish stop layer **14** adjacent to the trenches (Fig. 2).

A second layer **22** of a chemical mechanical polish resistant material is deposited conformally overall. The thickness of the second CMP resistant layer **22** is less than that of the first CMP resistant layer **14**.

The resulting structure is then partially planarized during the first step by first selectively removing the second CMP resistant layer **22** in the regions overlying the substrate surface layers **20** and narrower trenches **16** by chemical mechanical polishing with a known low-selectivity chemical mechanical polishing slurry, e.g. SS25 or SC-112 made by Cabot Corporation (Fig. 3). Selective removal can be achieved for example by using a high platen RPM and low spindle down force during the partial planarization step. Values of platen RPM would range from about 40 RPM to about 150 RPM, and down force values would range from about 2 PSI to about 7 PSI, but are not limited to these values.

The exposed dielectric 32 remaining in the regions overlying the substrate surface layers **20** and narrower trenches **16** after completion of the first polish step is planarized during the second polish step by removal with a known high selectivity slurry such as that made by Rodel or Solutions Technology, thus exposing the first polish resistant layer **14** (Fig. 4). A rinse or cleaning step can be incorporated to remove the bulk of the slurry remaining on the structure from the previous polish step, thus preventing cross-contamination of the different slurries.. Uniform removal is achieved using low platen speed and high down force. Values of platen RPM would range from about 10 RPM to about 50 RPM, and down force values would range from about 4 PSI to

about 11 PSI, but are not limited. Selectivity of oxide: nitride achieved with this type of slurry typically ranges from 15:1 to more than 200:1.

Material removal by a highly selective chemical mechanical polishing process provides a dielectric layer surface **42** adjacent to the substrate surface layer **20** having a surface which is coplanar to the surface of the first CMP resistant layer **44** and the step height differential between the dielectric layer surface **42** adjacent to the substrate surface layer **20** being determined primarily by the combined thickness' of the first CMP resistant layer 14 and the stress relief layer **12** (Fig. 4).

Additionally, the highly selective second CMP process step eliminates erosion of the second CMP resistant layer **46** remaining in the wider trench regions which results in elimination of dishing and CMP-related micro defects in these regions. This selective second process step also protects the wider trench regions from chemical etching during post-CMP cleaning steps which may incorporate dilute hydrofluoric acid (Fig. 4).

The remaining material comprising the first polish stop layer **14** and second polish stop layer **46** are then selectively removed down to the stress relief layer **52** or the level of the semiconductor substrate **20** as required (Fig. 5). (Fig. 4).

Further processing would typically comprise removal of the stress relief layer **20** (Fig. 4) and regrowth of a high-quality gate dielectric **60** on the semiconductor substrate **20** (Fig. 5) followed by deposition and lithographic patterning of the gate electrode **62** (Fig. 6).

Typically, trench dielectric isolation layers comprise 0.3 to 0.7 μm of a layer of dielectric such as silicon dioxide which may be formed by chemical vapor deposition, or by a composite process including step of thermal oxidation preceding or following a deposition process. A layer of silicon nitride, about in the range of 200 to 800 Å thick provides a suitable chemical mechanical polish resistant layer, although other polish stop layers can be utilized.

In a typical process utilizing, for example, a Strasbaugh CMP tool for this invention, the process flow would be as follows:

1. transfer wafers to table 1;
2. polish wafers on table 1 using low selectivity slurry and high speed, low-down force process conditions: 15 to 60 sec, approx.;
3. transfer wafers to a rinse station or to a third polish platen for DI rinsing or buff polish;
4. transfer wafers to table 2;

5. polish wafers on table 2 using high selectivity slurry using low-speed, high down force process conditions: 30 to 180 sec, approx.;

Option A:

6. transfer wafers to table 3 (optional);

7. polish wafers using DI, soft pad (optional): 30 sec, approx.;

Option B:

6. transfer wafers to a rinse station or to a third polish platen for DI rinsing or buff polish

7. transfer wafers back to table 1;

8. polish wafers using low selectivity slurry: 15 to 60 sec, approx.

Other variations in the polish sequence can be applied to this process to produce a final planar surface appropriate to the IC process being used.

The present invention can be carried out in a variety of commercially available polishing tools. The specific application is novel and should be tailored to meet the various conditions of the tool. In a process utilizing, for example, an Applied Materials Mirra CMP tool for this invention, the process flow would be as follows:

1. polish wafers on table 1 using low selectivity slurry, at high table speed and low down force: 15 to 60 sec, approx.;
2. polish wafers on table 2 using high selectivity slurry, low speed and high down force: 30 to 90 sec, approx.;
3. polish wafers on table 3 using high selectivity slurry, low speed and high down force: 30 to 90 sec, approx.

Alternatively, the third table on the Mirra system could be used for a final DI water polish process on a soft pad. Optimization of the process on this tool for high throughput may dictate other variations in the process.

In a typical process utilizing, for example, the Speedfam Auriga CMP tool for this invention, the process flow would be as follows:

1. polish wafers on table 1 using low selectivity slurry, low speed and high down force: 15 to 60 sec, approx.;
2. polish wafers on table 2 using high selectivity slurry, low speed and high down force: 30 to 180 sec, approx.

Other variations in this process for all tools mentioned above might include, for example, polishing wafers on a single table using the low selectivity slurry, and switching to a high selectivity slurry on the same table while continuing to polish the wafers. Yet another

variation on this process would be using a hard pad on the first table, and soft pad on the second table. Variations due to different tool configurations may be required without departing from the scope of the invention. As merely an example, U.S. Serial No.08/892,795 in the name of Walsh et al., which is commonly assigned, and hereby incorporated by reference describes yet another tool where the present invention can be implemented.

Although the description above were in terms of selected CMP tools, it would easily be recognized that other tools may also be used. Additionally, the tools described are merely illustrations and should not limit the scope of the claims herein. It would even be conceivable that multiple tools could be utilized or dedicated to specific process steps if multiple polish tables were not available on a single tool. One of ordinary skill in the art would recognize other variations, alternatives, and modifications.

In a method of forming an integrated circuit according to another embodiment, as shown in Figs. 7 to 10, a substrate for an integrated circuit is provided in the form of a first interlayer dielectric **70** (ILD), as shown in Fig. 7.

Conductive regions **71** are defined on the ILD layer e.g. by a conventional photoengraving step involving deposition of the conductive layer, coating with photoresist, and patterning. Wide separations **72** and narrow separations **73** are created upon removal of the conductive material **71** during the above-mentioned patterning step.

Subsequently a conformal layer **74** of a dielectric material or combination of materials is deposited overall. The thickness of the dielectric material or combination of materials is such that the surface **76** of the dielectric material **74** in the wide separation region **72** is higher than the surface **75** of the conductive material **71**. The dielectric comprises for example a conformal layer of CVD silicon dioxide.

A layer **77** of a chemical mechanical polish resistant material is deposited conformally overall.

The resulting structure is then partially planarized during the first step by first selectively removing the CMP resistant layer **77** in the regions overlying the conductive layers **71** by chemical mechanical polishing with a known low-selectivity chemical mechanical polishing slurry, e.g. SS25 or SC-112 made by Cabot Corporation. Selectivity of oxide: nitride achieved with this type of slurry typically ranges from 15:1 to more than 200:1.(Fig. 8).

The exposed dielectric **80** remaining in the regions overlying the conductive layers **71** after completion of the first polish step (Fig. 8) is planarized during

the second polish step by removal with a known high selectivity slurry such as that made by Rodel or Solutions Technology until the surface **90** of the polish resistant layer **77** is coplanar with the resultant surface **92** of the planarized dielectric (Fig. 9). Selectively of oxide:nitride achieved with this type of slurry typically ranges from about 15:1 to more than 200:1.

The highly selective second CMP process step eliminates erosion of the CMP resistant layer **90** remaining in the wider spaced regions 72 regions which results in elimination of dishing and CMP-related micro defects in these regions.

Alternatively, a hard polish pad can be used on the first table during the second polish step, eliminating the need for a high-speed, low down force process in this first step.

The remaining material comprising the polish resistant layer **90** is then selectively removed (Fig. 10).

Experiments

To prove the principles and operation of the present inventions, experiments have been performed. These experiments are merely examples of how the present invention has been used. One of ordinary skill in the art would recognize numerous variations, alternatives, and modifications. Accordingly, the present experiments should not be construed as limiting the scope of the present invention in any manner.

Figs. 11-14 show a simplified pictorial of the experimental procedure according to an embodiment of the present invention. Fig. 11 (11A-11B) show a simplified sequence of steps performed in the experimental procedure. Starting substrates were 150 mm, (100) orientation 13-17 ohm-cm p-type silicon wafers. The isolation mask was prepared by depositing a 120 nm LPCVD nitride film on 15nm thermal pad oxide. After definition of the isolation windows using a standard photolithographic step, the isolation mask was etched by a magnetically-enhanced reactive ion etch (MERIE) system until the silicon substrate was exposed. Subsequently, 0.68 μm deep trenches in the substrate silicon were formed using HBr/Cl_2 plasma etch in a MERIE etch system. After cleaning, the trenches were refilled using a 720 nm PECVD undoped TEOS oxide oxyannealed at 850°C and a blanket, 40 nm thick, LPCVD nitride overcoat deposition

(Fig. 11A). The wafers were planarized by removing the excess oxide using CMP process conditions listed in Table 1 (Fig. 11B).

PARAMETER	STEP 1
Platen RPM	100
Carrier RPM	50
Pressure (PSI)	3
Pad	IC1000 on SUBA IV
Slurry	SC-1, 2:1
Slurry Flow (sccm)	175
Pad Temperature (Deg.C)	40
Polish Time (minutes)	2, 4, 5, 6, 8

TABLE 1: CMP conditions

This was followed by a standard chemical clean, and by a wet nitride strip (Figs. 11C and 11D). Samples were prepared from at least 8 different areas on a wafer representing a variety of structures and areas that combine the worst-case polishing scenarios (i.e. very large and small high features and very large, low features). The final structure after gate electrode formation is shown in Fig. 11E, which was acceptable.

Fig. 12 is the mask layout used to determine both dishing and planarization characteristics as a function of the polish process conditions. It is typical of an ASIC-type design and contains both dense as well as very sparse, active areas. This is considered one of the "worst case" layouts for planarization using the CMP technique. Substantially no dishing was observed in any low region with polish times of less than 6 minutes, and

minimal dishing (e.g., less than 20 nm) was observed in very large, low features after an 8 minute polish. Planarization of high features is weakly dependent upon the feature size but, in all cases, active device regions were planarized after a 6 minute polish. Polish rates in the active device regions rapidly approached zero after the nitride polish stop was exposed (Fig. 13) and planarization was achieved. This is likely related to (a) the relative hardness of the nitride polish stop layer compared to oxide, (b) lack of topography, which reduces slurry transport to the salient regions, and, (c) enhanced pad deconditioning due to the high speed, low pressure process. This last effect is demonstrated in Fig. 14, in which the low speed, high pressure process continues to remove material beyond 8 minute polish time, while the high speed, low pressure process removes material at approximately 1/4 of the rate until about 6 minutes, at which time the removal rate drops to zero. For ease of interpretation, the incremental effect of this planarizing technique was evaluated by SEM micrographs of trenches with different geometries were taken for different polish times. Cross-sections for both a dense SRAM region, as well as a large isolated active region, showed excellent planarization to the polish stop, and exhibit self-limiting polish characteristics. These features were planarized using the high speed, low pressure polish process and show that the nitride overcoat is rapidly removed from high features, but remains intact in the very wide low regions for polish times of up to 5 minutes.

Small features are planarized more quickly than large features, as expected, but the polish rate is reduced to near zero upon reaching the nitride polish stop and achieving planarization. Larger features which have not yet been planarized continue to be removed until the polish stop is reached and planarity is achieved. The polish rate in these features is also reduced to near zero at this point. This phenomenon allows larger features to "catch up" with the faster-polishing smaller features and is akin to a highly selective etch process that can tolerate a range of thicknesses across a wafer. More importantly, this allows the planarization process to be "self stopping". In low features greater than 60 μm in width, the nitride overcoat is consumed from the center to the edge during polishing. For very wide regions, the clearing edge exclusion area (where the nitride remains after the central region has been cleared) is very small relative to the size of the feature (less than ~30 μm) and the overcoat is consumed uniformly across the feature except for the exclusion area.

The self-stopping process is related to a number of issues. The first issue is the relative hardness of the polish stop layer with respect to the layer being planarized.

The process will, automatically slow down as the faster-polishing oxide layer is eventually consumed, and the nitride layer becomes the bulk of the surface being polished. The second issue involves the reduction of slurry transport which occurs with the lack of topography when planarization is achieved. The third issue is related to enhanced pad deconditioning caused by the high speed process.

The high speed, low pressure process allows planarization of very large regions of dense topography (e.g., of at least up to 2 x 3 mm^2) and very large isolated features such as a substrate capacitor (e.g., of at least up to 1.1 x 1.1 mm^2) without causing dishing of very wide low regions or significantly thinning the nitride polish stop layer. This has the advantage of determining what the height of the trench isolation region will be above the device well immediately after planarization. This step height can be tailored by changing the nitride polish stop thickness and trench fill deposition thickness appropriately. In order to optimize the STI process, the appropriate nitride polish stop and pad oxide thickness must be optimized to produce enough step height differential between the device well and field regions to planarize disparate feature sizes simultaneously, as well as be thin enough after CMP planarization such that post-clean step height can be minimized. The trench fill and planarization processes are decoupled, giving the advantage of greatly improved process control, because the final field thickness essentially depends only upon the trench depth and trench fill deposition thickness. Other factors, not related to planarization, which will affect the final field thickness are the nitride polish stop thickness in the active area, the post-CMP cleaning strategy, and the pre-gate oxide etchback process. Since the shallow trench isolation process does not produce the "white ribbon effect" associated with LOCOS processes, less aggressive or no pre-gate processing can be implemented thus simplifying the gate formation process. These factors lead to a very robust STI technique.

Dishing and planarization characteristics as a function of polish time for the high speed, low pressure polish process on various feature geometries were discussed. No dishing was observed in any low region with polish times < 6 minutes. It has been successfully demonstrated a simple shallow trench global planarization technique in which planarization of high features is only weakly dependent upon feature size and device well regions were planarized after a 6 minute polish. It was shown that polish rates in active regions rapidly approached zero after the nitride polish stop was exposed and, as a result, topography was effectively planarized without dishing, independently of feature size. The planarization process was concluded without significant thinning of the

nitride polish stop layer. This allows for the optimization of the STI process by choosing the appropriate nitride polish stop and pad oxide thickness to produce the required step height differential between the device well and field regions for correct active transistor operation. It also allows the planarization process to be decoupled from the trench etch and fill process leading to a very robust STI process. The above experiment is merely an illustration and should not limit the scope of the claims herein in any manner. One of ordinary skill in the art would recognizes other variations, alternatives, and modifications.

Although particular embodiments of the invention have been described in detail, it should be appreciated that numerous modifications, variations and adaptations may be made without departing from the scope of the invention as defined in the embodiments. In particular, while the above description is in terms of planarizing an isolation structure, it can also be applied to a metal damascene structure made of materials such as copper, aluminum, gold, and the like. Additionally, the planarizing technique can also be applied to fabrication of other films such as metals, aluminum, gold, copper, and the like in integrated circuits. Furthermore, the present invention can be expanded to cover the techniques described in the Appendix.

WHAT IS CLAIMED IS:

1. A method of fabricating an integrated circuit, comprising:

providing a semiconductor substrate having a surface and having formed thereon a surface layer of a stress relief material and an overlying layer of a first chemical mechanical polish resistant material, the substrate having defined therein a trench;

filling the trench with at least one layer of dielectric material overlying the layer of the first chemical mechanical polish resistant material, the thickness of the dielectric material being sufficient to fill the widest trench region to a level above the substrate surface layer;

forming a second layer of a chemical mechanical polish resistant material overlying the layer of dielectric material, the thickness of the second layer of chemical mechanical polish resistant material being less than the thickness of the first layer of chemical mechanical polish resistant material;

partially planarizing the second layer of chemical mechanical polish resistant material using a first CMP step by selective removal of the chemical mechanical polish resistant material overlying the semiconductor substrate not subtended by the trench regions and exposing the underlying dielectric layer in those regions using a low selectivity slurry whereby the second layer of chemical mechanical polish resistant material overlying the semiconductor substrate in the trench regions remains essentially intact to provide a polish stop layer in those regions; and

planarizing the exposed dielectric layer using a second CMP step by selective removal of the dielectric material overlying the semiconductor substrate not subtended by the trench regions and exposing the first chemical mechanical polish resistant material using a high selectivity slurry whereby the second layer of chemical mechanical polish resistant material overlying the semiconductor substrate in the trench regions prevents dishing of the trench filling material and prevents micro scratching of the trench filling material underlying the second layer of chemical mechanical polish resistant material.

2. A method of fabricating an integrated circuit, comprising:

providing a semiconductor substrate having a surface and having formed thereon conductive regions with both wide and narrow separations;

forming a layer of dielectric material overlying the conductive regions, the thickness of the dielectric material being sufficient such that the surface of the dielectric

material in the wide separation region is higher than the surface of the conductive material;

forming a conformal layer of a chemical mechanical polish resistant material overlying the layer of dielectric material;

partially planarizing the second layer of chemical mechanical polish resistant material using a first CMP step by selective removal of the chemical mechanical polish resistant material overlying the conductive regions and exposing the underlying dielectric layer in those regions using a low selectivity slurry whereby the layer of chemical mechanical polish resistant material overlying the separation regions between the conductive regions remains essentially intact to provide a polish stop layer in those regions;

planarizing the exposed dielectric layer using a second CMP step by selective removal of the dielectric material overlying the conductive regions using a high selectivity slurry whereby the second layer of chemical mechanical polish resistant material overlying the semiconductor substrate in the separation regions prevents dishing of the dielectric material and prevents micro scratching of the dielectric material underlying the second layer of chemical mechanical polish resistant material.

3. A method for planarizing a film of material in the manufacture of a device, said method comprising:

providing a semiconductor substrate having a surface and having formed thereon conductive regions with both wide and narrow separations;

forming a layer of dielectric material overlying the conductive regions, the thickness of the dielectric material being sufficient such that the surface of the dielectric material in the wide separation region is higher than the surface of the conductive material;

forming a conformal layer of a chemical mechanical polish resistant material overlying the layer of dielectric material;

partially planarizing on a first CMP table the second layer of chemical mechanical polish resistant material using a first CMP step by selective removal of the chemical mechanical polish resistant material overlying the conductive regions and exposing the underlying dielectric layer in those regions using a low selectivity slurry whereby the layer of chemical mechanical polish resistant material overlying the

separation regions between the conductive regions remains essentially intact to provide a polish stop layer in those regions;

planarizing on a second CMP table the exposed dielectric layer using a second CMP step by selective removal of the dielectric material overlying the conductive regions using a high selectivity slurry whereby the second layer of chemical mechanical polish resistant material overlying the semiconductor substrate in the separation regions prevents dishing of the dielectric material and prevents micro scratching of the dielectric material underlying the second layer of chemical mechanical polish resistant material.

4. The method of claim 3 wherein said first CMP table is different from said second CMP table.

5. The method of claim 4 wherein said first CMP table and said second CMP table are provided on a CMP apparatus.

6. The method of claim 4 wherein said first polish step comprises a high-speed, low-down force polish process on a stacked polish pad consisting of a hard upper pad overlying a soft lower pad.

7. The method of claim 4 wherein said first polish step comprises a low speed, high down force polish process on a hard pad and said second polish step comprises a low speed, high down force polish process on a soft pad.

8. A method of fabricating an integrated circuit, comprising:

providing a semiconductor substrate having a surface and having formed thereon conductive regions with both wide and narrow separations;

forming a layer of dielectric material overlying the conductive regions, the thickness of the dielectric material being sufficient such that the surface of the dielectric material in the wide separation region is higher than the surface of the conductive material;

planarizing the layer of dielectric material overlying the conductive regions;

forming trenches in the layer of dielectric material;

forming openings in the trenches which expose the underlying conductive layer forming a second conformal conductive layer, filling the openings and trenches previously formed;

forming a conformal layer of a chemical mechanical polish resistant material overlying the second conductive layer of material;

partially planarizing the second layer of chemical mechanical polish resistant material using a first CMP step on a first polish platen by selective removal of the chemical mechanical polish resistant material overlying the dielectric regions and exposing the underlying second conductive layer in those regions using a low selectivity slurry whereby the layer of chemical mechanical polish resistant material overlying the trench regions remains essentially intact to provide a polish stop layer in those regions;

planarizing the exposed second conductive layer using a second CMP step on a second polish platen by selective removal of the dielectric material overlying the conductive regions using a high selectivity slurry whereby the layer of chemical mechanical polish resistant material overlying the semiconductor substrate in the separation regions prevents dishing the conductive material underlying the layer of chemical mechanical polish resistant material.

9. The method of claim 8 wherein said planarizing of the exposed second conductive layer also prevents microscratching of the conductive material underlying the layer of chemical mechanical polish resistant material.

10. A method for planarizing a film of material on a substrate structure, said method comprising:

providing a substrate comprising a top surface and a film to be polished overlying said top surface;

removing a first portion of said film using a first polishing table; and

removing a second portion of said film using a second polishing table to selectively remove said second portion of said film relative to said top surface;

wherein said first polishing table and said second polishing table are provided on a common platform.

11. The method of claim 10 wherein said first portion of said film is removed using a selective polishing material and said second portion of said polishing film is removed by a non-selective polishing material.

12. The method of claim 10 wherein said top surface comprises a flat planar region and a recessed region, which underlies said flat planar region.

13. The method of claim 10 wherein said first portion of said film is removed using a non-selective polishing material and said second portion of said polishing film is removed by a selective polishing material.

14. The method of claim 10 wherein said top surface is from a film of silicon material.

15. The method of claim 1 wherein said top surface is from a film of dielectric material.

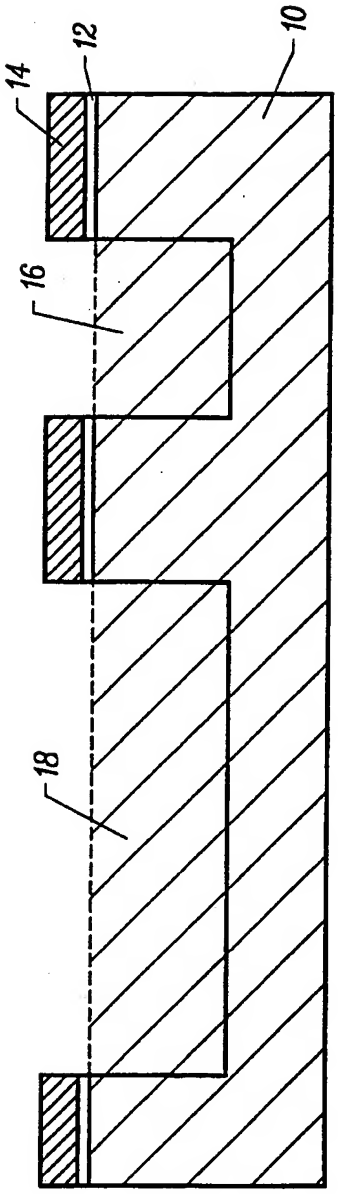


FIG. 1

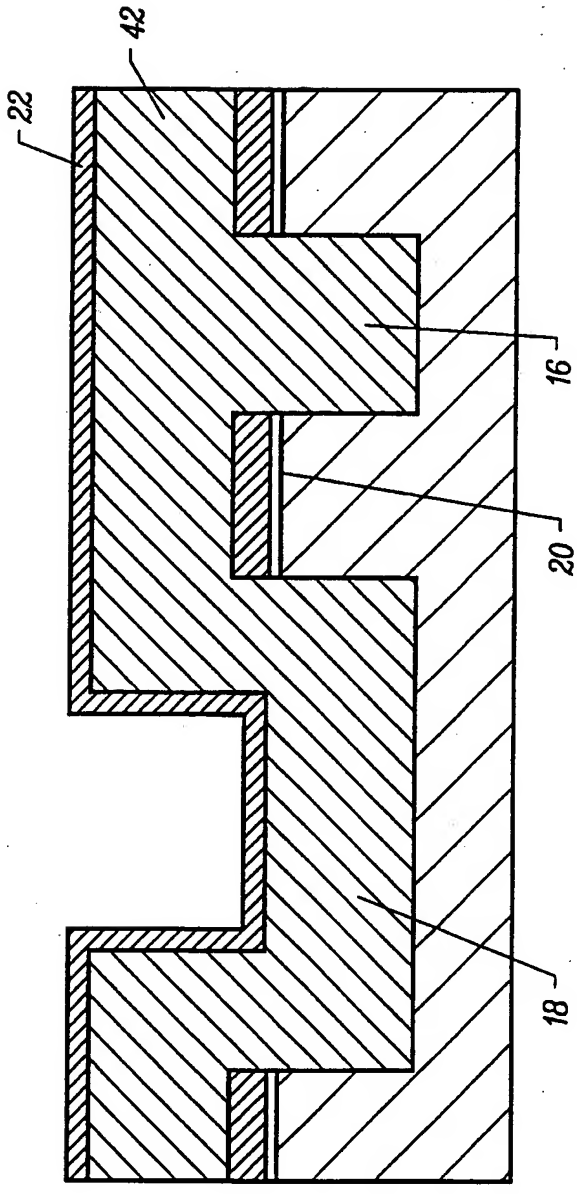


FIG. 2

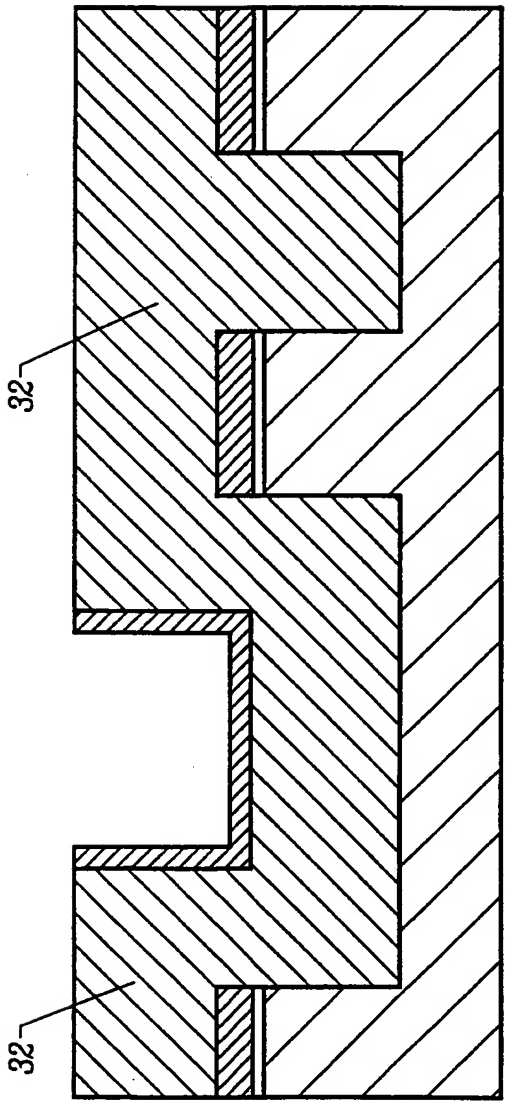


FIG. 3

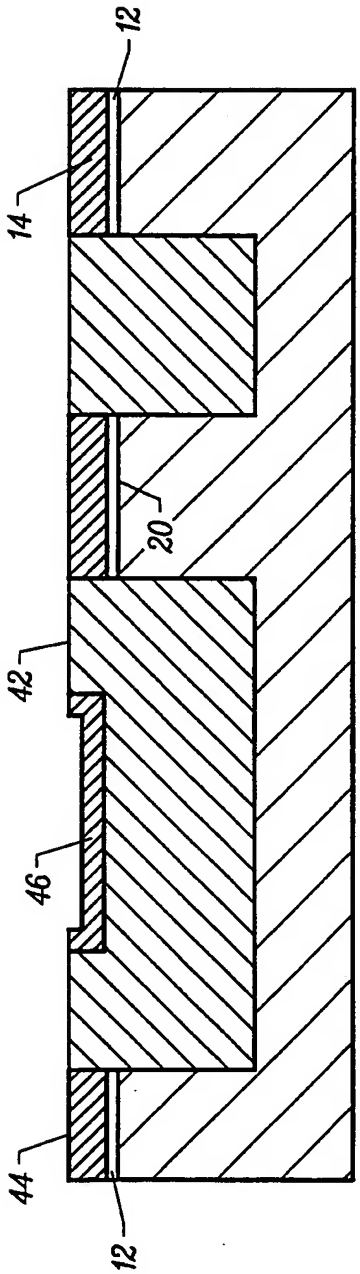


FIG. 4

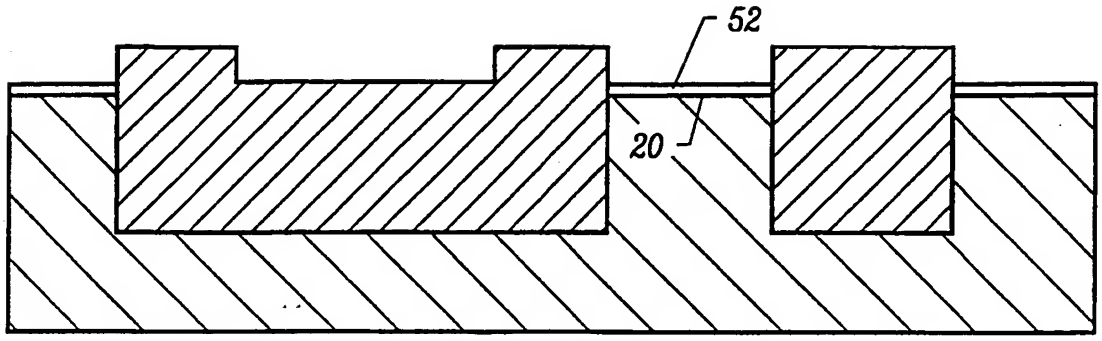


FIG. 5

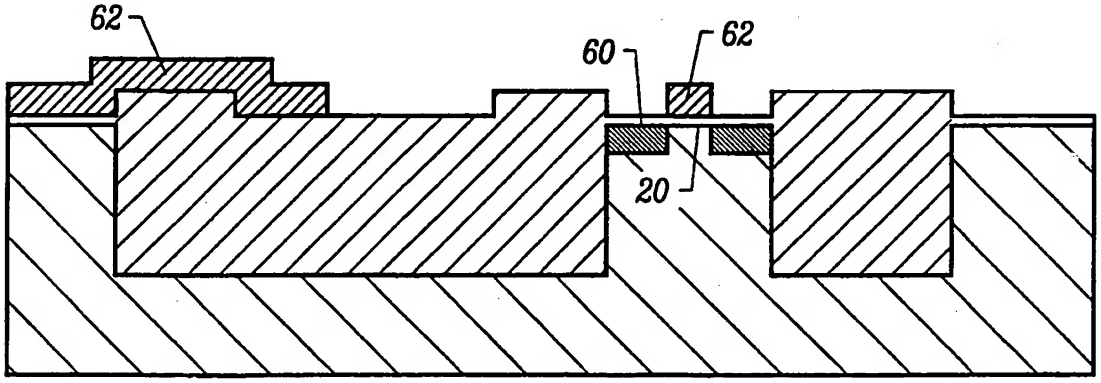


FIG. 6

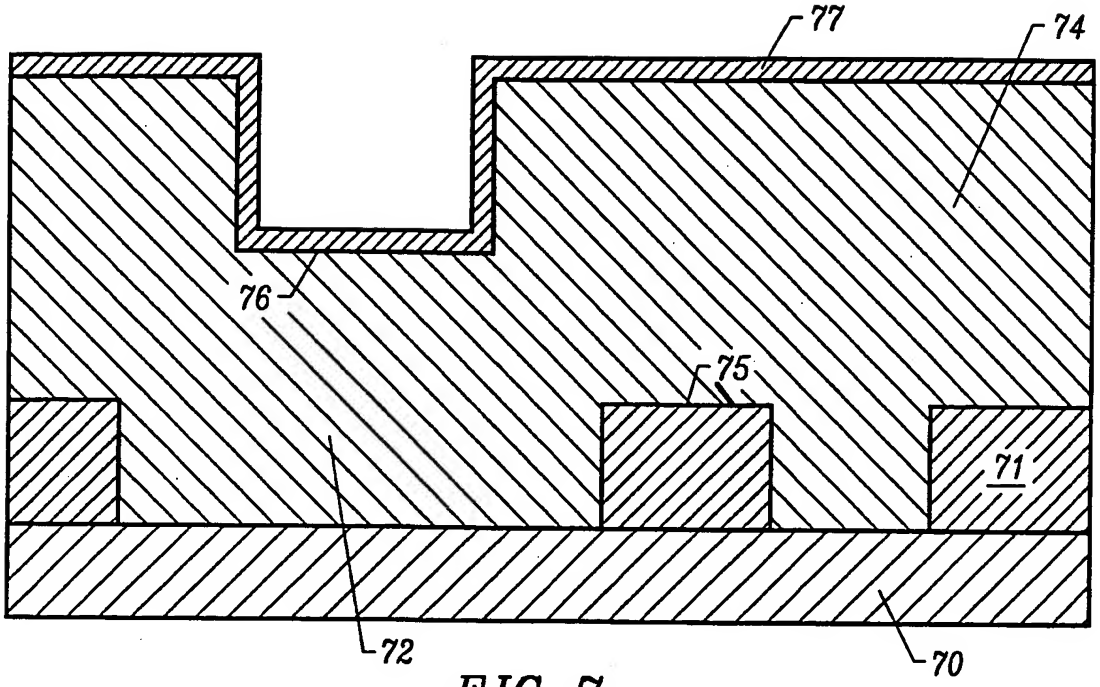


FIG. 7

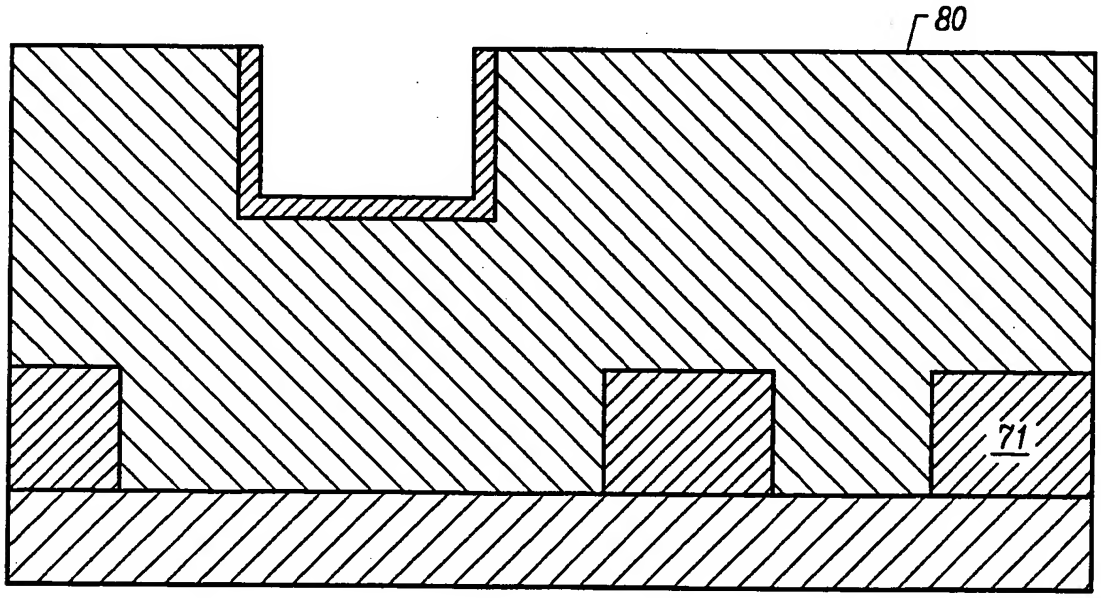


FIG. 8

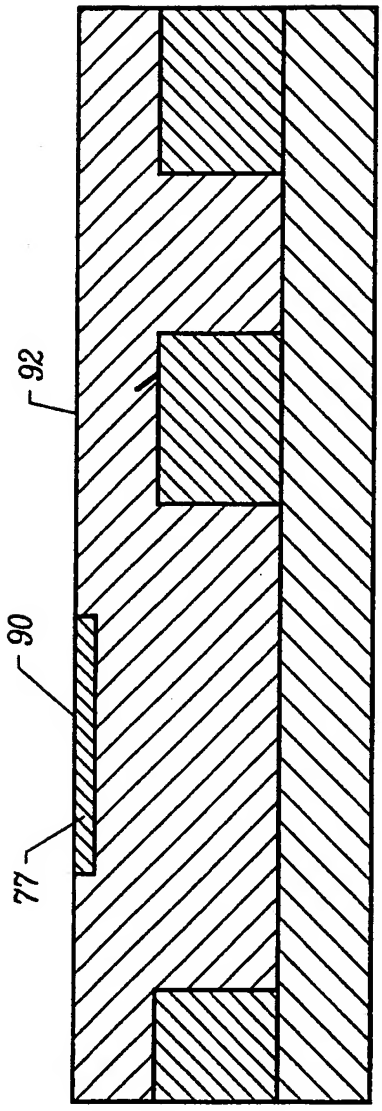


FIG. 9

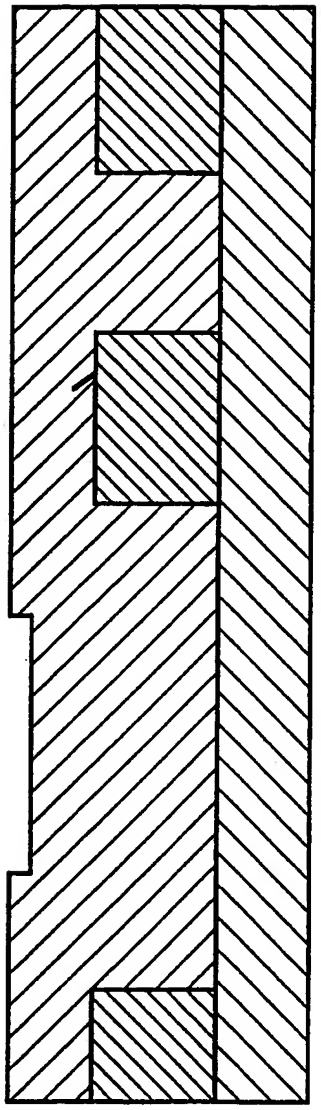
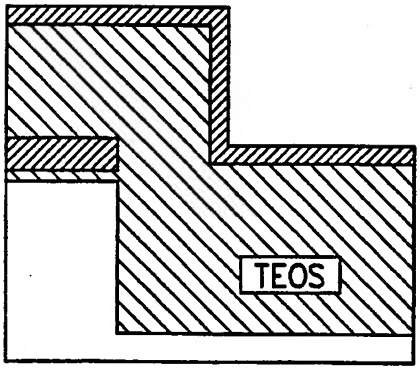
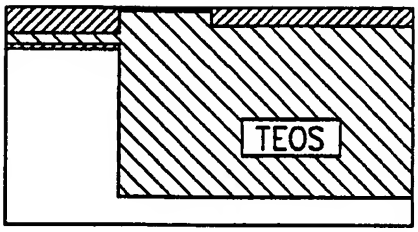


FIG. 10



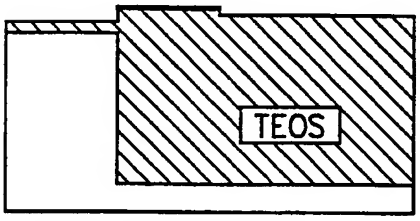
STI trench fill + overcoat

FIG. 11A



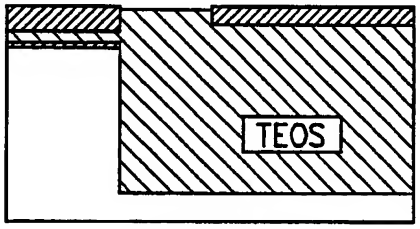
CMP + over-polish

FIG. 11B



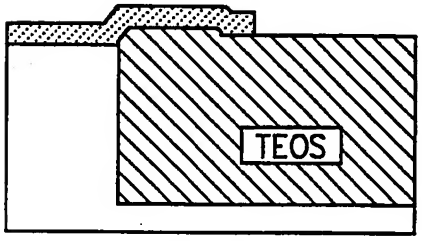
wet nitrite strip

FIG. 11D



post-CMP clean

FIG. 11C



pregate & gate formation

FIG. 11E

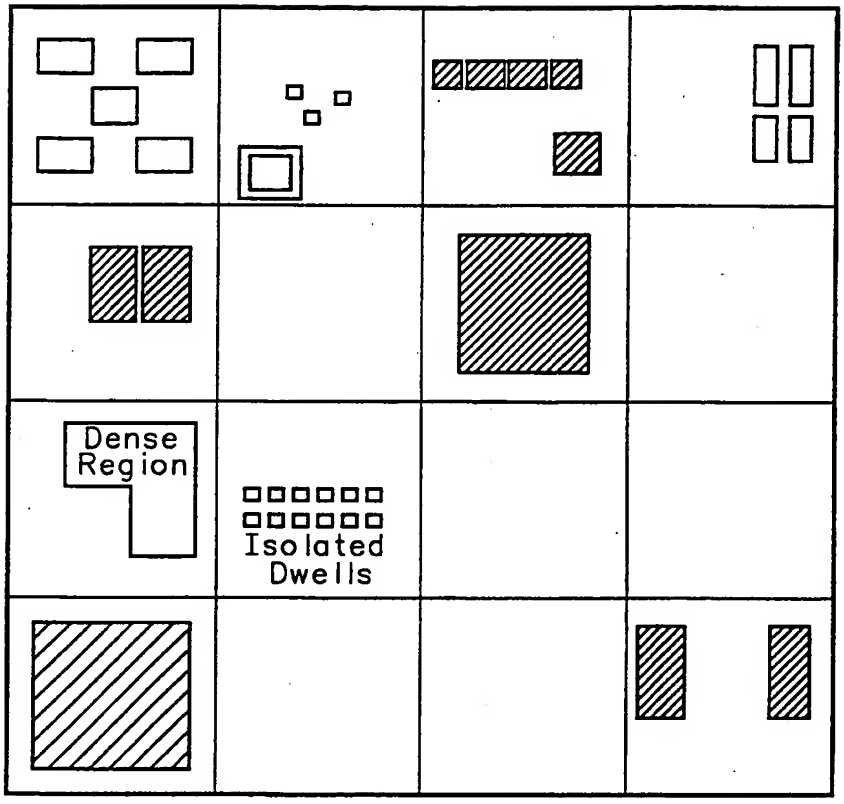


FIG. 12

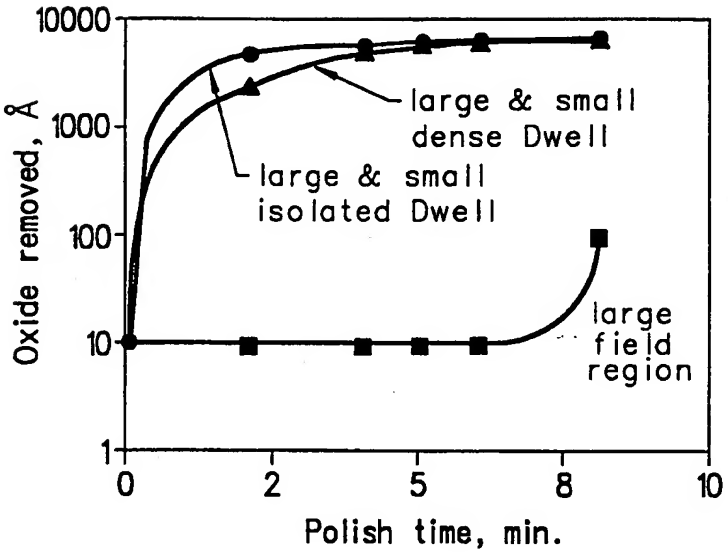

10000
1000
100
10
1
Oxide removed, Å
large & small
dense Dwell
large & small
isolated Dwell
large
field
region
0
2
5
8
10
Polish time, min.

FIG. 13

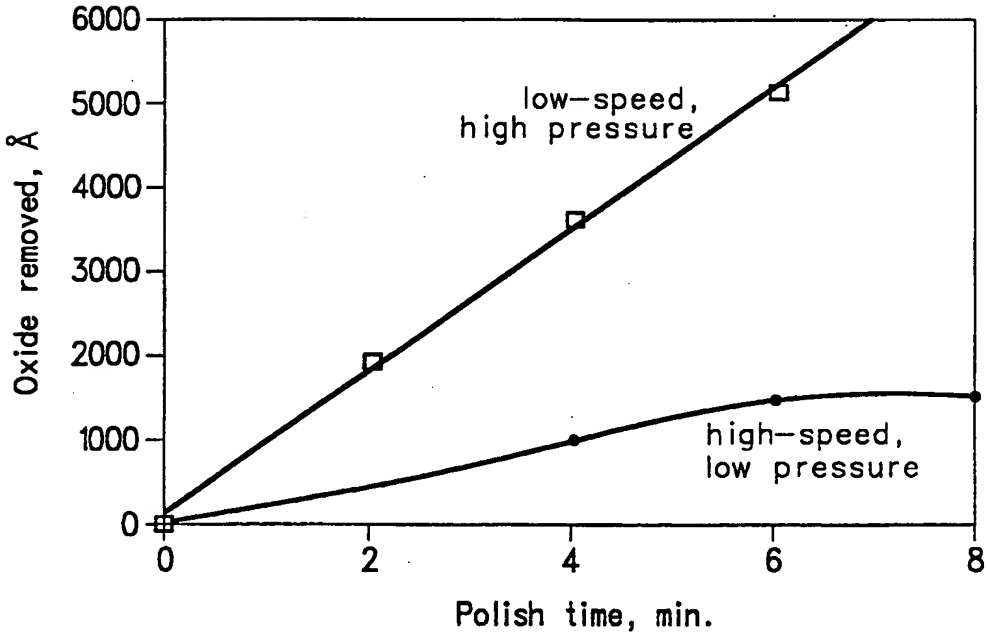

6000
5000
4000
3000
2000
1000
0
Oxide removed, Å
low-speed,
high pressure
high-speed,
low pressure
0
2
4
6
8
Polish time, min.

FIG. 14

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/05192

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :B24B 7/22, 23/02; B24C 1/04, 1/08
US CL : 438/633, 634, 645, 692, 740 ; 451/285, 287, 288
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 438/633, 634, 645, 692, 740 ; 451/285, 287, 288

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

none

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
Search terms: cmp, etch### (3a) (resist### or stop or rate)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,663,107 A (Peschke et al) 02 September 1997, col. 4, line 18 - col. 5, line 19.	1-15
P	US 5,817,567 A (Jang et al) 06 October 1998, col. 2, line 29- col. 3, line 18.	1-15
Y	US 5,362,669 A (Boyd et al) 08 November 1994, col. 3, line 4-col. 4, line 65.	1,10-15
Y	US 5,721,172 A (Jang et al.) 24 February 1998, col. 7, line 28-col. 18, line 25.	1-15
Y	US 5,665,202 A (Subramanian et al) 09 September 1997, col. 4, line36-col. 6, line 30.	1-15

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search	Date of mailing of the international search report
06 MAY 1999	25 MAY 1999
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer HA NGUYEN Telephone No. (703) 308-2706

Form PCT/ISA/210 (second sheet)(July 1992)*